Polybus Systems Corporation

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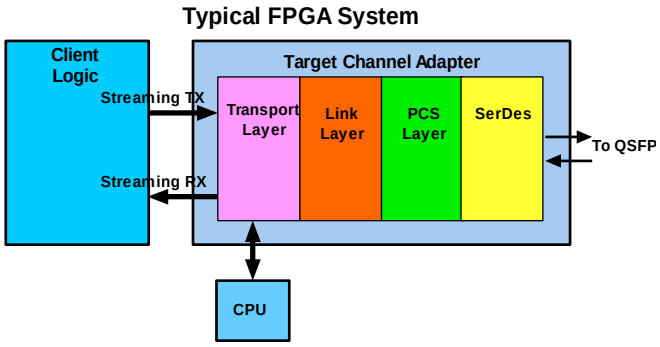
InfiniBand Cores from Polybus Systems

Polybus offers a family of InfiniBand Cores ranging from Single Data Rate 4X (10Gb/Second) to Quad Data Rate 4X (32Gb/Sec in FPGAs). All Link Layer cores and Target Channel Adapter cores are available for Altera FPGAs.

Link Layer Cores are fully compliant with the IBTA 1.2.1 standard, providing auto-negotiation, link layer flow control, CRC generation and checking and link layer format checking. Link Layer Cores are designed for very low latency operation and wire speed bandwidth.

Target Channel Adapters combine a Link Layer Core with a UC Transport Layer core. TCAs support UC SEND and UC RDMA and UD SEND services. TCAs provide 32 to 1024 Queue Pairs and one to eight Virtual Lanes (depending on application requirements and FPGA resources). The high speed data connections are simple FIFO interfaces that are easily connected to the streaming interfaces supported by Altera.

Polybus InfiniBand cores are interoperable with all Mellanox and QLogic switches and HCAs.



Applications

- Target Channel Adapters and Bridges,

  Polybus InfiniBand Cores are developed in partnership with Tenesix, Inc. 20 Taylor St. Littleton, MA 01460.
- SPI4 -> InfiniBand
- FibreChannel -> InfiniBand
- High speed data acquisition (Video, Radar ...)
- Routers and Switches

Custom Application Support

Polybus Systems and Tenesix Inc, will provide custom core development, integration support, and system verification support.

Target Channel Adapters

- 20GBit/second (DDR), 40GBit/second (QDR)
- Unreliable Connect SEND and RDMA Write
- Unreliable Datagram SEND (in QDR TCA only)
- QDR TCA supports both cutthrough and store and forward modes.
- 1024 Queue Pairs
- Unlimited 2 Gbyte Unreliable Requests
- Single or multiple data lanes
- 64 bit Transmit and Receive DMA Interface for DDR, 128 bit interfaces for QDR.
- IBA Version 1.2.1 compatible
- Supports Altera Stratix 5
- 270MHz clock

DDR 4X InfiniBand Link Layer Core

- 20 Gbit/second
- 64 bit parallel interfaces
- 1X, 4X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1, 2 & 4 Virtual Lanes
- Supports Stratix5GX
- Very low latency
- IBA Rev 1.2.1 compliant
- Supports Altera Stratix 5,
- Proven design, running in FPGAS and ASICs
- 250MHz clock

QDR 4X/8X Link Layer Core

- 80 Gbit/second in ASICs
- 40 Gbits/second in FPGA
- 128 bit parallel interfaces
- 1X, 4X, 8X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1,4 & 8 Virtual lanes.
- Very low latency
- IBA Rev 1.2.1 compliant
- Supports Altera Stratix 5
- Proven design, running in ASICs and FPGAs
- 270MHz (FPGA), >500MHz ASICs

	UC DDR TCA QDR		QDR Link Layer 8VLs		UC QDR TCA	
FPGA		S5GX		S5GX		S5GX
VLANES		2		8		2
MHz		250		300		300
LEs		18,832		27,447		36,658
Flip Flops		22546		23273		39,912
BRAMS		1,233,472 Bits		48,039 Bits		1,536,807 Bits