Polybus Systems Corporation

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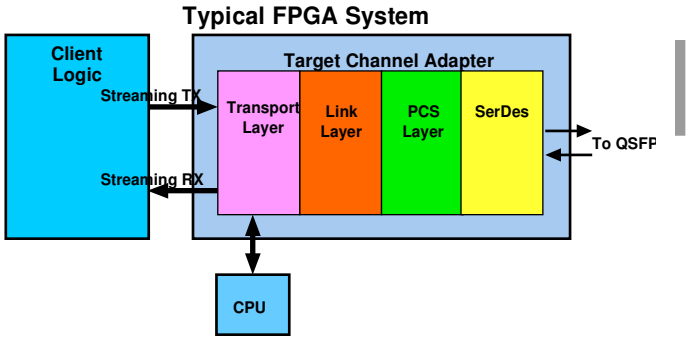
InfiniBand Cores from Polybus Systems

Polybus offers a family of InfiniBand Cores ranging from Single Data Rate 4X (10Gb/Second) to Quad Data Rate 4X (32Gb/Sec in FPGAs). All Link Layer and Target Channel Adapter cores are available for the Xilinx 7 Series FPGAs.

Link Layer Cores are fully compliant with the IBTA 1.2.1 standard, providing auto-negotiation, link layer flow control, CRC generation and checking and link layer format checking. Link Layer Cores are designed for very low latency operation and wire speed bandwidth.

Target Channel Adapters combine a Link Layer Core with a UC Transport Layer core. TCAs support UC SEND and UC RDMA and UD SEND services. TCAs provide 32 to 1024 Queue Pairs and one to eight Virtual Lanes (depending on application requirements and FPGA resources). The high speed data connections are simple FIFO interfaces that are easily connected to the AXI4 streaming interfaces Xilinx.

Polybus InfiniBand cores are interoperable with all Mellanox and QLogic switches and HCAs.



Applications

- Target Channel Adapters and Bridges,
- P(Polybus InfiniBand Cores are
- 1(developed in partnership with Tenesix, Inc. 20 Taylor St. Littleton,
- HMA 01460.
- SPI4 -> InfiniBand
- FibreChannel -> InfiniBand
- High speed data acquisition (Video, Radar ...)
- Routers and Switches

Custom Application Support

Polybus Systems and Tenesix Inc, will provide custom core development, integration support, and system verification support.

DDR and QDR Target Channel Adapters

- 16GBit/second (DDR), 32GBit/second (QDR)
- Unreliable Connect SEND and RDMA Write
- Unreliable Datagram SEND (in QDR TCA only)
- QDR TCA supports both cutthrough and store and forward modes.
- 1024 Queue Pairs
- Unlimited 2 Gbyte Unreliable Requests
- Single or multiple data lanes
- 64 bit Transmit and Receive DMA Interface for DDR, 128 bit interfaces for QDR.
- IBA Version 1.2.1 compatible
- Supports Virtex7 and Kintex7.
- 270MHz clock

QDR 4XLink Layer Core

- 32 Gbits/second in FPGA
- 128 bit parallel interfaces
- 1X, 4X, 8X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1,4 & 8 Virtual lanes.
- Very low latency
- IBA Rev 1.2.1 compliant
- Supports Xilinx Virtex7 and Kintex7.
- Proven design, running in ASICs and FPGAs
- 270MHz (FPGA),

	UC DDR TCA QDR 2VLs		QDR Link Layer 8VLs		UC QDR TCA 2VLs	
FPGA	Kintex7		Kintex7		Kintex7	
VLANES	2		8		2	
MHz	250		260		260	
LUTS	12962		16717		26015	
Flip Flops	14480		16502		29857	
BRAMS	11 RAMB18 34 RAMB36		0		17 RAMB18 48 RAMB36	