



## Polybus Systems Corporation

23 Providence Rd  
Westford, MA 01886  
(978) 692-4828  
bjrosen@polybus.com

### InfiniBand Link Layer Cores from Polybus Systems

Polybus offers a family of InfiniBand Link Layer Cores ranging from a Single Data Rate 4X core (10Gbit/Second) to a Quad Data Rate 8X core (80Gbit/second). All Link Layer cores are available for both Xilinx and Altera FPGAs as well as for ASIC applications.

There are three members of the Link Layer family. The SDR Link Layer Core is the smallest core, it operates at 125 MHz and supports bidirectional speeds of 10Gbits/second in each direction. Customers are currently using the SDR core in Xilinx Virtex2P, Xilinx Virtex4FX, Altera Stratix2GX and ASICs. The SDR core can operate in the lowest speed grades of the Virtex4FX (-10) and the Stratix2GX (-5).

The DDR (Double Data Rate) Link Layer Core operates at 250 MHz and supports bidirectional speeds of 20Gbits/second. The DDR core requires a 5 GHz SerDes. Customers are using the DDR core in Xilinx Virtex4FX, Altera Stratix2GX and in ASICs. The DDR core requires the middle speed grades of the the Virtex4FX (-11) and the Stratix2GX (-4).

The newest member of the Polybus core family is the QDR (Quad Data Rate) Link Layer Core. The QDR cores supports 8X operation at DDR speeds (40Gbits/Second) in FPGAs at 250 MHz and 8X QDR speeds (80Gbits/Second) at 500 MHz in ASICs. The QDR core requires the highest speed grade Stratix2GX (-3). The RTL for the QDR core is available now, it is targeted at the Virtex5FXT and Stratix3 families which should be available in Q3 2007.

### Applications

- Target Channel Adapters and Bridges,
- PCI -> InfiniBand
- 1G, 10G Ethernet -> InfiniBand
- HyperTransport -> InfiniBand
- SPI4 -> InfiniBand
- FibreChannel -> InfiniBand
- High speed data acquisition (Video, Radar ...)
- Routers and Switches

### Custom Application Support

Polybus Systems and Tenesix Inc, will provide custom core development, integration support, and system verification support.



Polybus InfiniBand Cores are developed in partnership with Tenesix, Inc. 20 Taylor St. Littleton, MA 01460.

## SDR 4X InfiniBand Link Layer Core

- 10 Gbit/second
- 64 bit parallel interfaces
- 1X, 4X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1, 2 & 4 Virtual lanes
- Supports internal and external SerDes.
- Very low latency
- Fully portable, FPGA and ASIC compatible.
- IBA Rev 1.1 compatible
- Supports Xilinx Virtex2P, Virtex4FX-10 and Altera Stratix2GX
- Proven design, shipping in FPGAS and ASICs
- 125MHz clock

## DDR 4X InfiniBand Link Layer Core

- 20 Gbit/second
- 64 bit parallel interfaces
- 1X, 4X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1, 2 & 4 Virtual Lanes
- Supports Xilinx, Altera and ASIC SerDes
- Very low latency
- Fully portable, FPGA and ASIC compatible.
- IBA Rev 1.2 compatible
- Supports Xilinx Virtex4FX-11, Altera Stratix2GX-4.
- Proven design, running in FPGAS and ASICs
- 250MHz clock

## QDR 8X InfiniBand Link Layer Core

- 80 Gbit/second in ASICs
- 128 bit parallel interfaces
- 1X, 4X, 8X operation
- Link initialization and training
- Link layer flow control
- CRC generation and checking
- Protocol error and packet length checking
- Programmable Flow Control Period
- Dynamic Flow Control Mechanism
- Available for 1,4 & 8 Virtual lanes.
- Supports Xilinx, Altera and ASIC SerDes.
- Very low latency
- Fully portable, FPGA and ASIC compatible.
- IBA Rev 1.2 compatible
- Supports Altera Straitx2GX-3 and Xilinx Virtex5FXT when available
- 250MHz/500MHz clock

SDR Link Layer 4VLs			DDR Link Layer 4VLs			QDR Link Layer 8 VLs		
	V4FX			V4FX	S2GX		V4FX	S2GX
LUTS	5880		LUTS	6825	8161	LUTS	13,280	20200
Flip Flops	3659		Flip Flops	5807	5444	Flip Flops	10,368	12022
RAM Bits	0		RAM Bits	0	3872	RAM Bits	192	8344