

UC Transport Layer Core

- 10Gbit/second
- Unreliable Connect SEND and RDMA Write
- 1024 Queue Pairs
- Unlimited 2 Gbyte Unreliable Requests
- Single or multiple data lanes
- 64 bit Transmit and Receive DMA Interfaces
- IBM DCR interface (Xilinx PPC compatible)
- IBA Version 1.2 compatible
- Supported in the Virtex2p, Virtex4FX, Virtex5 and Stratix2GX FPGAs,

RC Transport Layer Core

- 10Gbit/second
- Reliable and Unreliable Connect SEND, RDMA Write and Reliable Connect RDMA READ
- 1024 Queue Pairs
- Uses DDR2 RAMs for RC Retry Memory
- 511 Reliable Requests in flight at any one time
- Up to 1 MByte Reliable Request size depending on DDR2 memory size.
- Unlimited 2 Gbyte Unreliable Requests
- End to End Flow Control
- Single or multiple data lanes
- 64 bit Transmit and Receive DMA Interfaces
- IBM DCR interface (Xilinx PPC compatible)
- IBA Version 1.2 compatible
- Supported in the Virtex2p, Virtex4FX and Virtex5

DDR Transport Layer Core

- 20Gbit/second
- Unreliable Connect SEND and RDMA Write
- 1024 Queue Pairs
- Unlimited 2 Gbyte Unreliable Requests
- Single or multiple data lanes
- 64 bit Transmit and Receive DMA Interfaces
- IBM DCR interface (Xilinx PPC compatible)
- IBA Version 1.2 compatible
- Supported in the Virtex5FXT and Stratix2GX

Target Channel Adapter FPGA resource utilization

| | UC SDR TCA | | RC SDR TCA | | UC DDR TCA | | SDR Dual Port TCA | |
|-------------------|--------------|--------------------|--------------|---------------|--------------|-------------|-------------------|--|
| | V4FX | S2GX | V4FX | V4FX | V5 | S2GX | V4FX | |
| FPGA | V4FX | S2GX | V4FX | V4FX | V5 | S2GX | V4FX | |
| VLANES | 1 | 1 | 1 | 4 | 2 | 2 | 1 | |
| MHz | 125 | 125 | 125 | 125 | 250 | 250 | 125 | |
| LUTS | 11923 | 9866 | 18,004 | 19,274 | 11822 | 12349 | 18975 | |
| Flip Flops | 8585 | 10059 | 11,621 | 12,102 | 12765 | 15831 | 12788 | |
| BRAMS | 47 RAMB16 | 170 M4K 10 M512 | 80 RAMB16 | 104 RAMB16 | 34 RAMB36 | 291 M4Ks | 97 RAMB16 | |